

IN THE CLAIMS:

Please cancel claims 1-20, amend claims 21 and 24-26 and add new claims 27-37 as follows. Please note that claims 22-23 remain unchanged, but are reproduced for the Examiner's convenience and reference.

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1 21. (Amended) A method of fabricating an integrated circuit comprising[
2 the steps of]:
3 depositing a field implant;
4 depositing a well implant; and
5 depositing an enhancement implant, wherein the [steps of] depositing a field
6 implant, depositing a well implant, and depositing an enhancement implant are done using a
7 single mask.

25-29
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33-37

1 22. (Unchanged) The method of claim 21 wherein the well implant is an n-
2 well implant.

1 23. (Unchanged) The method of claim 21 wherein the well implant is a p-
2 well implant.

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1 24. (Amended) The method of claim 21 further comprising[the steps of]:
2 forming a high voltage native transistor by blocking the well implant and the
3 enhancement implant; and
4 offsetting the field implant from an active area of the native transistor, thereby
5 obtaining high gated-diode junction breakdown characteristics.

1 25. (Amended) The method of claim 21, further comprising[the step of]
2 implanting a pocket implant to improve a punch-through immunity.

1 26. (Amended) The method of claim 21 further comprising[the step of]:
2 depositing two pocket implants; and
3 merging the pocket implants together by lateral diffusion, whereby a channel
4 doping profile from the pocket implant diffusion exhibits reverse-short-channel effect.

Please add the following new claims:

1 --27. (New) A method of fabricating a transistor in integrated circuit device
2 comprising:
3 providing a semiconductor substrate;
4 forming a gate oxide on the semiconductor substrate;
5 forming a gate on the gate oxide;
6 implanting a first pocket implant into the semiconductor substrate from a first
7 side of the gate;
8 implanting a second pocket implant into the semiconductor substrate from a
9 second side of the gate; and
10 diffusing the first pocket implant and the second pocket implant laterally in the
11 semiconductor substrate.

1 28. (New) The method of claim 27 wherein the first pocket implant is in
2 contact with the second pocket implant.

1 29. (New) The method of claim 27 wherein the first pocket implant and the
2 second pocket implant are implanted at an angle.

1 30. (New) The method of claim 27 wherein the first pocket implant and the
2 second pocket implant are implanted using the gate as a mask.

1 31. (New) The method of claim 27 wherein the diffusing increases a reverse
2 short channel effect of the transistor.

1 32. (New) The method of claim 27 further comprising implanting an
2 enhancement implant in the semiconductor substrate.

1 33. (New) The method of claim 27 further comprising forming a source on
2 the first side of the gate and a drain on the second side of the gate, wherein the source and
3 drain are doped at a first polarity and the first pocket implant and the second pocket implant
4 are doped at a second polarity.